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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/023,172	02/13/1998	THOMAS J. HOLMAN	042390.P5659	6584

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BLAKELY SOKOLOFF TAYLOR  
 AND ZAFMAN  
 12400 WILSHIRE BOULEVARD  
 SEVENTH FLOOR  
 LOS ANGELES, CA 900251026

EXAMINER

VERBRUGGE, KEVIN

ART UNIT	PAPER NUMBER
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2188

23

DATE MAILED: 08/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Page

# Office Action Summary

Application No.

09/023,172

Applicant(s)

HOLMAN, THOMAS J.

Examiner

Kevin Verbrugge

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 16 June 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 15-31 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 15-31 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                  | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____  |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)         | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ | 6) <input type="checkbox"/> Other: _____                                    |

## **DETAILED ACTION**

### ***Continued Prosecution Application***

The request filed on 6/16/03 for a Continued Prosecution Application (CPA) under 37 CFR 1.53(d) based on parent Application No. 09/023172 is acceptable and a CPA has been established. An action on the CPA follows.

### ***Response to Amendment***

This non-final Office action is in response to the CPA request above and the accompanying Amendment C, paper #22, filed 6/16/03. This amendment canceled claims 1-14 and added new claims 15-31. Claims 15-31 are therefore pending.

### ***Double Patenting***

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 15-31 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 21-40 of copending Application No. 09/023170 and claims 18-30 of copending Application No. 09/023234. Although the conflicting claims are not identical, they are not patentably distinct from each other because the differences in the claims are immaterial.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 15 and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 5,357,621 to Cox.

Regarding claim 15, Cox discloses a serial architecture for memory module control.

Cox shows the claimed memory module controller control logic as MCL controller 13 and memory address control logic 21.

Cox shows the claimed memory bus in Fig. 1 as the bus connecting MCL system controller 11 with the memory modules.

He shows the claimed system memory controller as MCL system controller 11.

He shows the claimed first memory module as module 1, item 20. He shows the claimed first plurality of memory devices as memory blk 1 and memory blk 2.

He shows the claimed interfaces as the interfaces between the items mentioned above.

Regarding claim 26, Cox's memory devices are volatile.

\*\*\*\*\*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 15-17, 24, and 26 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent 5,790,447 to Laudon et al., hereinafter simply Laudon.

Regarding claim 15, Laudon discloses a high-memory capacity DIMM with data and state memory.

He does not explicitly show the claimed memory bus and system memory controller, but there are inherent in his system since a system memory controller is required to control all the memory modules and a memory bus is required to transmit the signals from the system memory controller to the memory modules.

He shows the claimed first memory module as DIMM 102 in Fig. 4, for example. He shows the claimed first plurality of memory devices as SDRAM chips D0-D17. He shows the claimed first memory module controller as the control circuitry on the DIMM, including state memory 106, address/control buffers 214 and 216, and clock driver 218.

He shows the claimed interfaces as the interfaces between the items mentioned above.

Regarding claim 16, Laudon shows the claimed clock generator as clock driver 218 in Fig. 4.

Regarding claim 17, Laudon's memory module control circuitry includes the claimed request handling logic to determine if an address on the bus is directed at that particular memory module.

Regarding claim 24, Laudon's memory module is a DIMM as claimed.

Regarding claim 26, Laudon's memory devices are volatile.

\*\*\*\*\*

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,357,621 to Cox.

Regarding claim 16, Cox does not disclose a clock generator on his memory modules. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the claimed clock generator to enhance control of the memory module and enable clocking the devices at a different rate than the memory bus.

Regarding claim 17, Cox's first memory module controller performs the claimed function of ignoring memory address requests that are not addressed to the memory devices on its memory module. He teaches that "Each memory module responds to a range of addresses that includes its starting address and its ending address" (column 1, lines 59-61).

\*\*\*\*\*

Claims 18-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,357,621 to Cox in view of 5,655,113 to Leung et al. and 5,036,493 to Nielsen.

Cox does not teach that his memory module controllers include the claimed power management unit to control power supplied to the memory devices.

However, Leung (column 4, lines 33-37) and Nielsen both disclose systems which reduce power consumption by reducing power to part or all of one or more memory modules.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include power management circuitry on the memory modules of Cox to control the power consumed by the modules. The particular method of reducing the power consumed by the modules is a matter design choice and would include all of the claimed options: reduce power to the individual memory devices, decouple the devices from the bus, alter the clock frequency, and disable the clock.

Claims 24, 25, and 27-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,357,621 to Cox.

Regarding claims 24 and 25, Cox does not teach that his memory modules are SIMMs, however it would have been obvious to one of ordinary skill in the art at the time



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the invention was made to use SIMMs and DIMMs since they were the predominant memory module types at the time of the invention.

Regarding claim 27, Cox does not mention any handshaking circuitry, however it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the claimed handshaking logic to improve communications between the memory module controller and the system memory controller.

Regarding claim 28, Cox does not disclose the claimed data handling logic, however it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the claimed data handling logic to convert the data into the format required by the memory devices if the memory devices required a different format from the system memory bus.

Regarding claim 29, Cox does not disclose the claimed writing buffer, however it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the claimed writing buffer to store data.

Regarding claim 30, Cox does not disclose the claimed address storage unit. However, once one was motivated to include a writing buffer as mentioned above, it would have been similarly obvious to include the attendant address buffer for the addresses of the stored data.

Regarding claim 31, Cox does not disclose the claimed read buffer, however it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the claimed read buffer to store data.

\*\*\*\*\*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 18-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,790,447 to Laudon et al. in view of 5,655,113 to Leung et al. and 5,036,493 to Nielsen.

Laudon does not teach that his memory module controllers include the claimed power management unit to control power supplied to the memory devices.

However, Leung (column 4, lines 33-37) and Nielsen both disclose systems which reduce power consumption by reducing power to part or all of one or more memory modules.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include power management circuitry on the memory modules of

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Laudon to control the power consumed by the modules. The particular method of reducing the power consumed by the modules is a matter design choice and would include all of the claimed options: operate the devices at a different voltage than the memory bus, reduce power to the individual memory devices, decouple the devices from the bus, alter the clock frequency, and disable the clock.

Claims 25 and 27-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,790,447 to Laudon.

Regarding claim 25, Laudon does not teach that his memory modules are SIMMs, however he mentions SIMMs at column 1, lines 21-40 and teaches there that "SIMM and DIMM are often used synonymously in the memory art". In any case, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a SIMM in Laudon's device for its attendant advantages, including its reduced complexity compared with DIMMs.

Regarding claim 27, Laudon does not mention any handshaking circuitry, however it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the claimed handshaking logic to improve communications between the memory module controller and the system memory controller.

Regarding claim 28, Laudon does not disclose the claimed data handling logic, however it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the claimed data handling logic to convert the data into the format required by the memory devices if the memory devices required a different format from the system memory bus.

Regarding claim 29, Laudon does not disclose the claimed writing buffer, however it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the claimed writing buffer to store data since Laudon does include an address buffer 214.

Regarding claim 30, Laudon includes an address storage unit as address buffer 214. Furthermore, once one was motivated to include a writing buffer as mentioned above, it would have been similarly obvious to include the attendant address buffer for the addresses of the stored data.

Regarding claim 31, Laudon does not disclose the claimed read buffer, however it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the claimed read buffer to store data since Laudon does include an address buffer 214.

**Conclusion**

The method claims are grouped and rejected with the apparatus claims because the steps of the method are met by the disclosure of the apparatus and methods of the reference(s) as discussed above.

Any inquiry concerning this or an earlier communication from the Examiner should be directed to Primary Examiner Kevin Verbrugge by phone at (703) 308-6663.

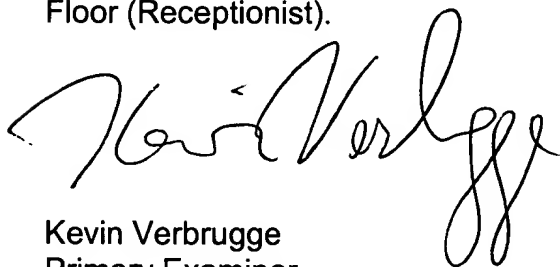
Any response to this action should be mailed to Commissioner for Patents, Washington, D.C. 20231 or faxed to

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and labeled appropriately (After-final, Official, Non-Official/Draft). Hand-delivered responses should be brought to Crystal Park 2, 2121 Crystal Drive, Arlington, VA, 4th Floor (Receptionist).



Kevin Verbrugge  
Primary Examiner  
8/20/03

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**IMPORTANT NOTICE**

The Examiner's art unit number has changed from 2187 to 2188 due to the recent realignment of workgroup 2180. Please use art unit 2188 on all correspondence related to this case.

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